

FIG. 1

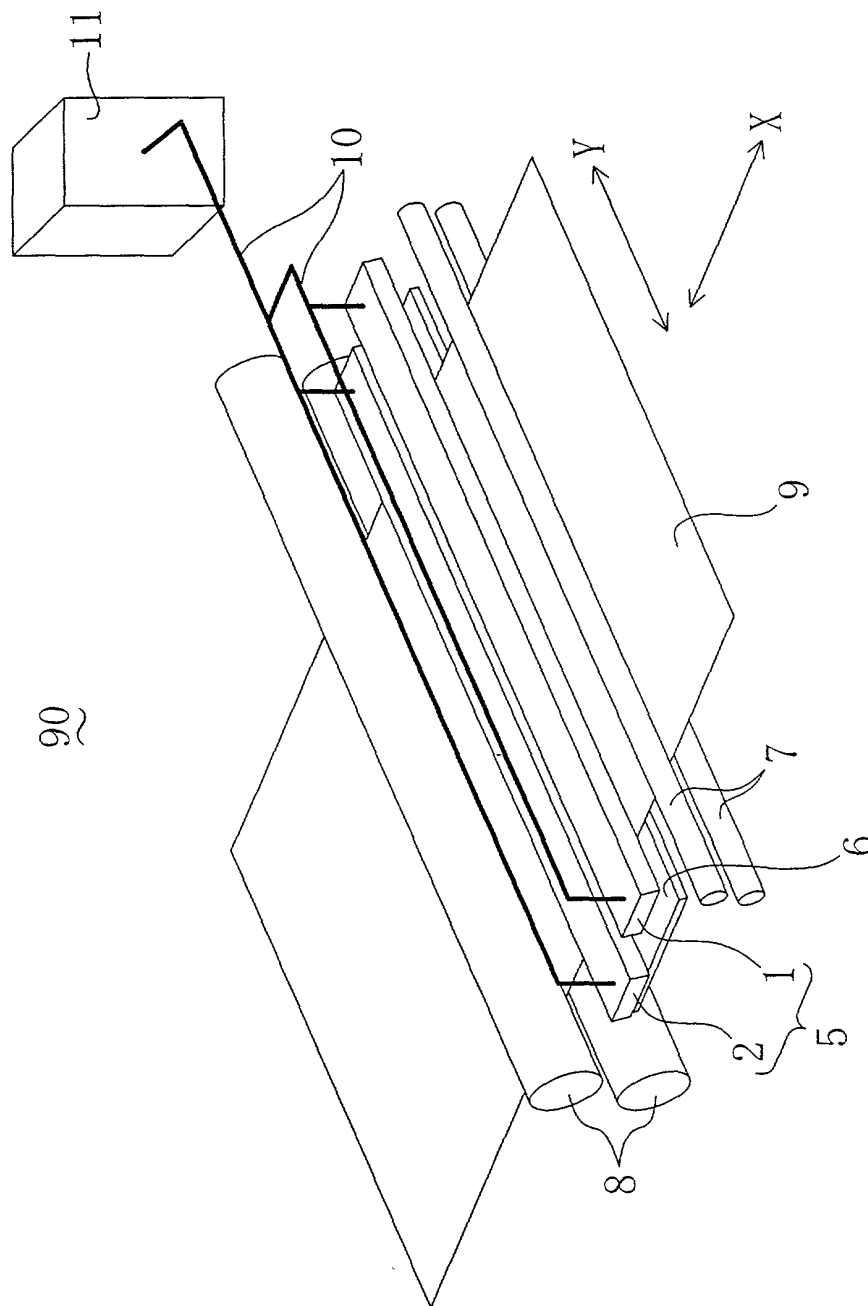


Figure 1 is a schematic diagram of a semiconductor device 100. The diagram includes a top view and a cross-sectional view. The top view shows a substrate 10 with a grid of electrodes 12 and 14. A central region 16 contains a patterned layer 15. A cross-sectional view 13 shows the vertical structure of the electrodes and the central region. A coordinate system (X, Y) is shown in the top right corner.

FIG. 3

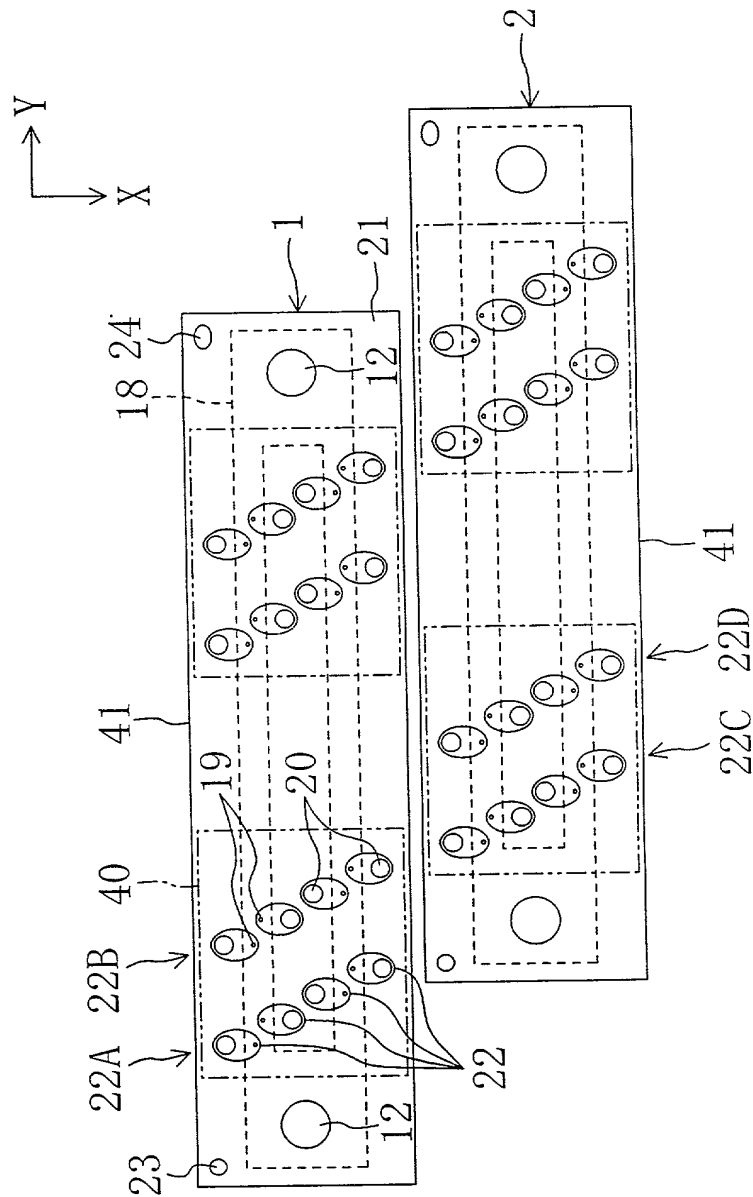


FIG. 4

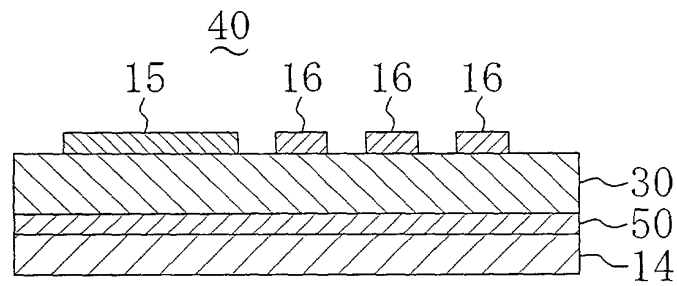


FIG. 5

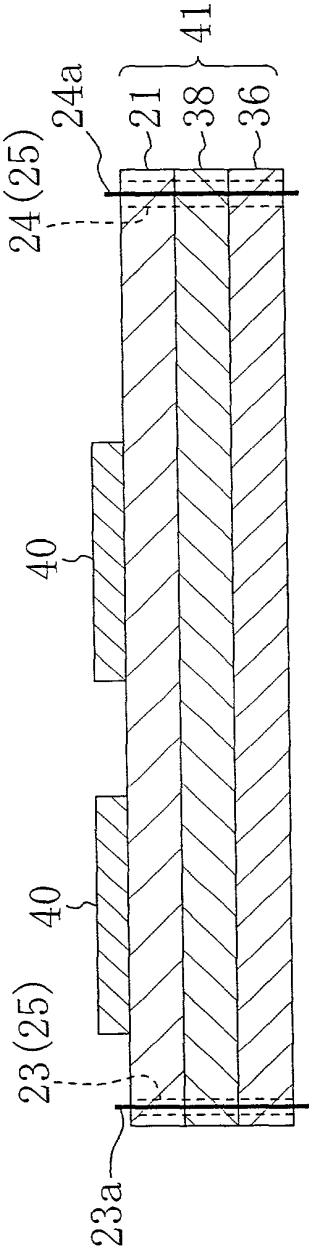


FIG. 6

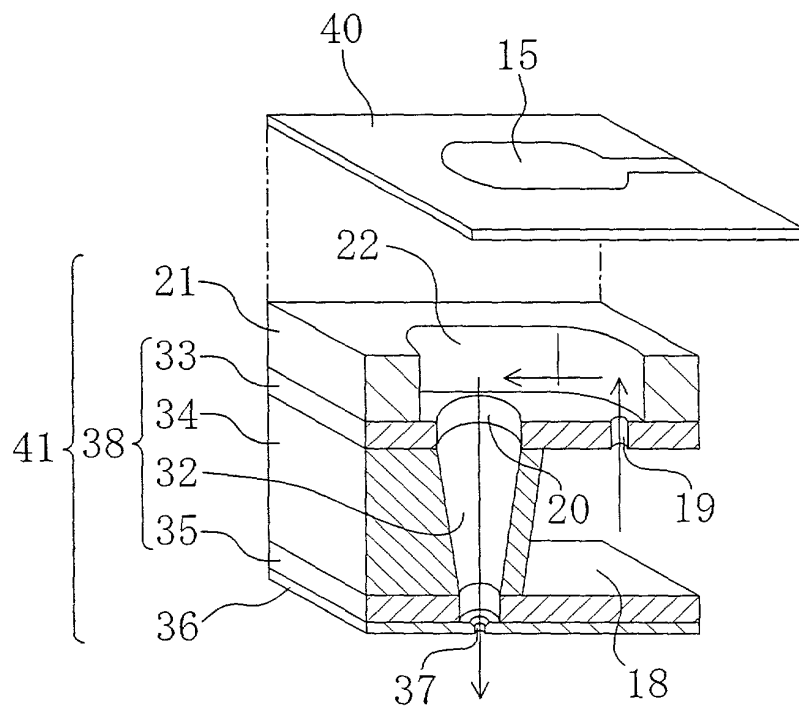


FIG. 7A

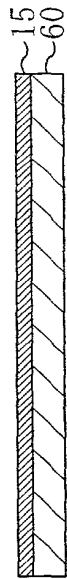


FIG. 7B

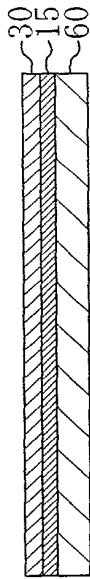


FIG. 7C

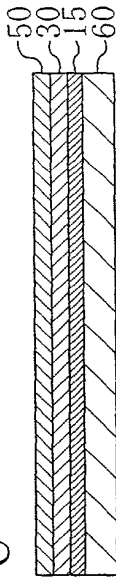


FIG. 7D

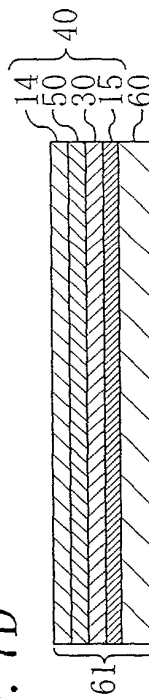


FIG. 7E

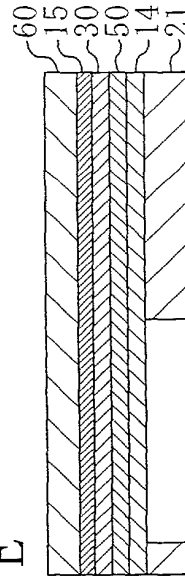


FIG. 7F

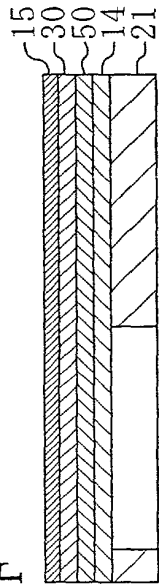


FIG. 7G

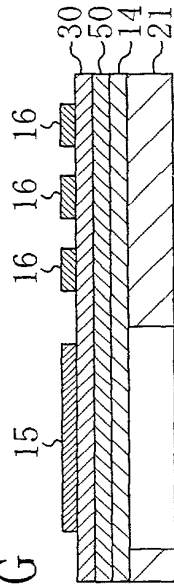


FIG. 7H

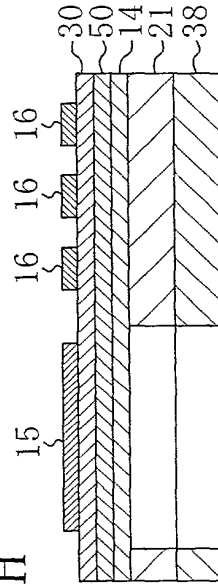


FIG. 7I

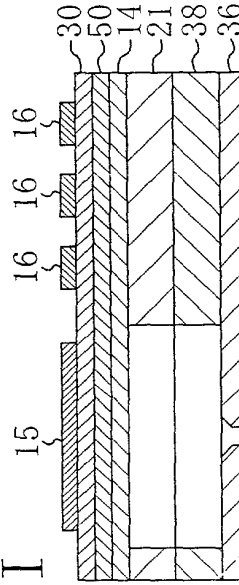


FIG. 8

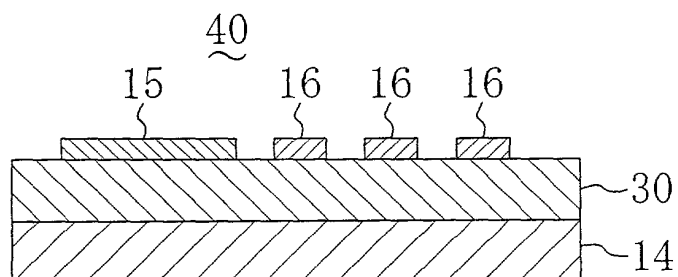


FIG. 9

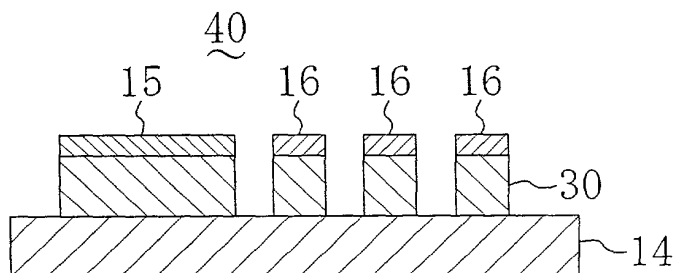


FIG. 10

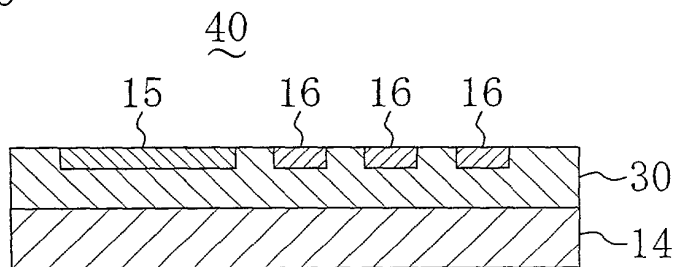


FIG. 11

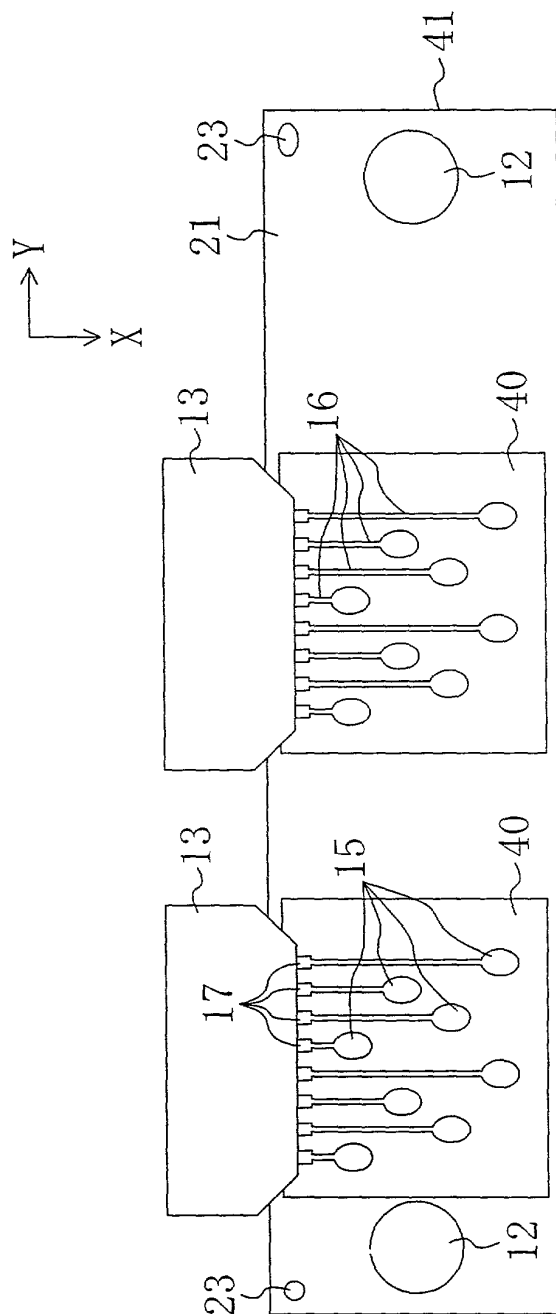
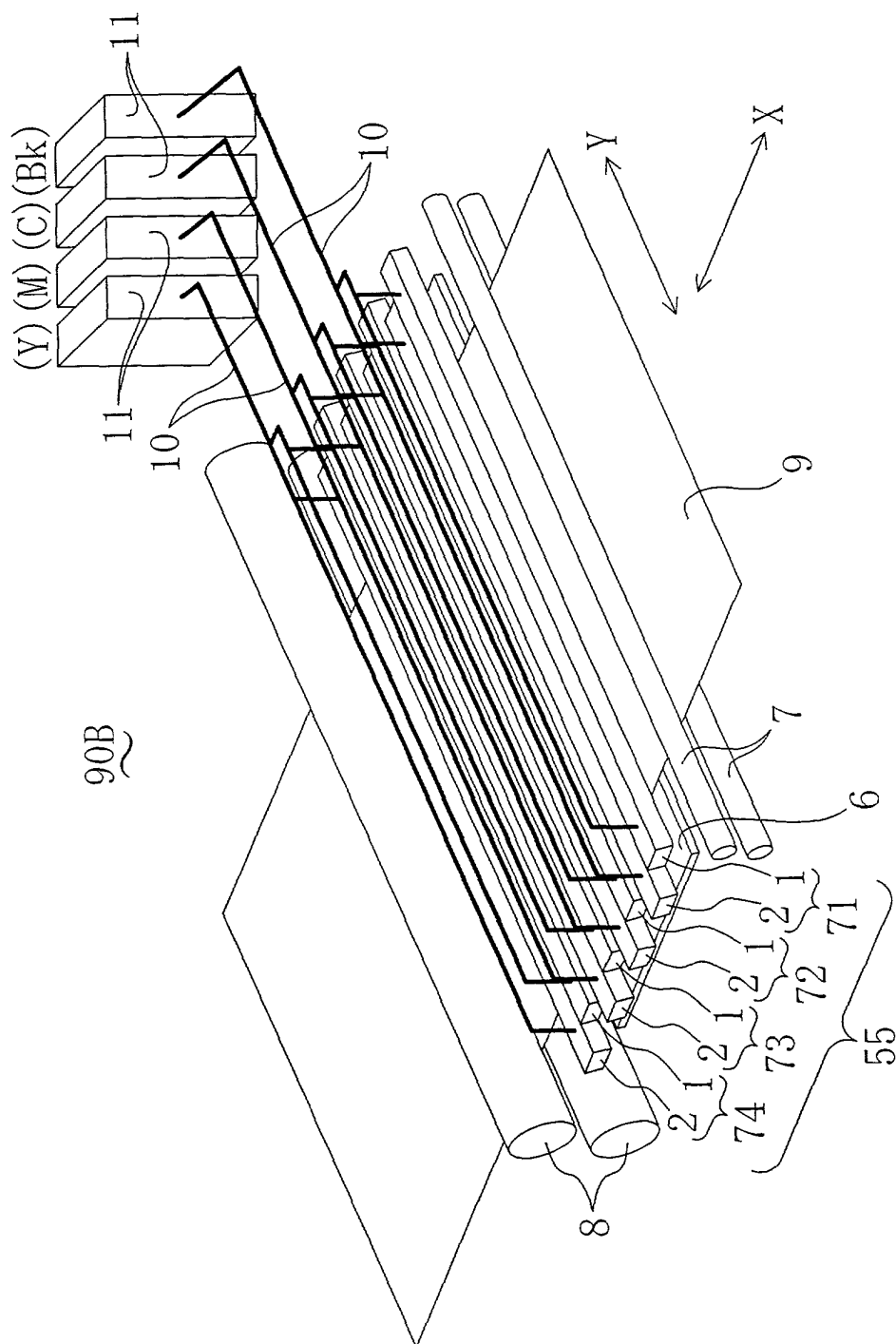
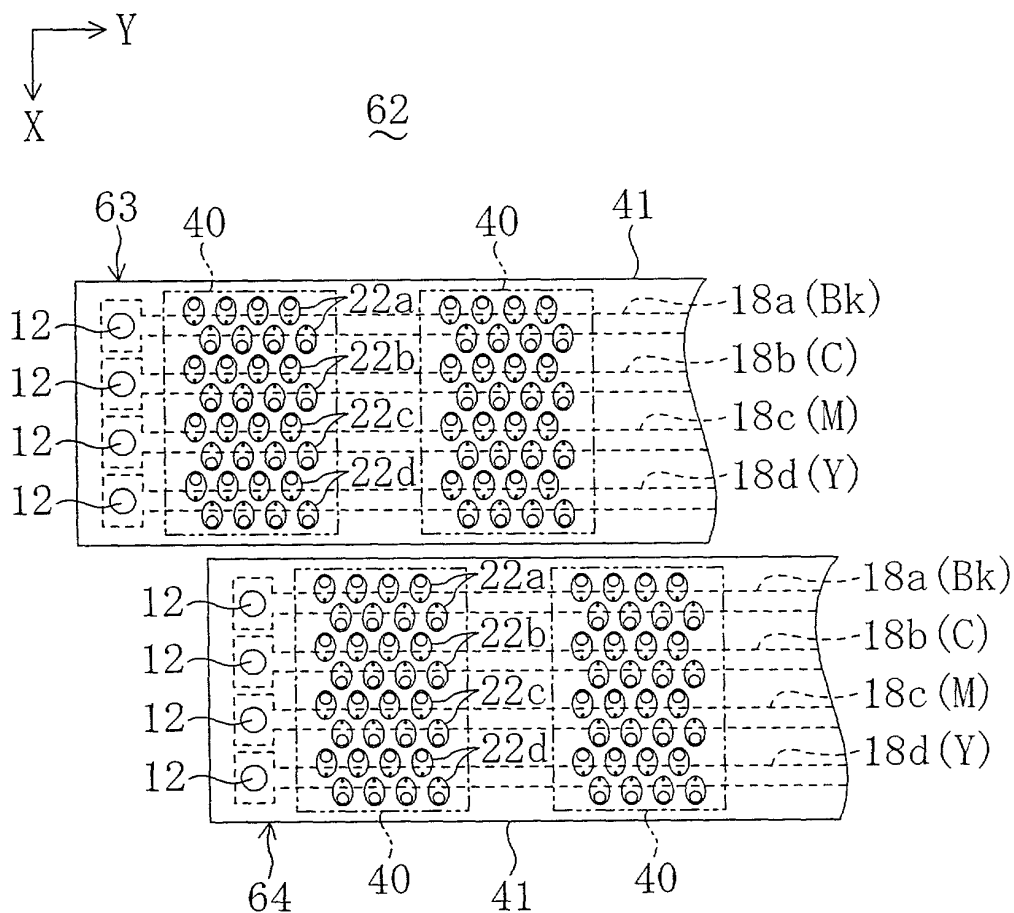


Figure 5A is a schematic diagram of a second embodiment of the device. It shows two parallel rectangular panels (12) connected by a central strip (23). Each panel (12) contains several internal regions (40) defined by dashed lines. These regions (40) contain particles (22), which are depicted as small circles with internal structures. The panels (12) are mounted on a base (24) via tabs (23). A coordinate system (X, Y) is shown at the top left, with the X-axis pointing right and the Y-axis pointing up. Labels 22A and 22B are used to indicate specific regions within the panels (12).





[illegible]

FIG. 16

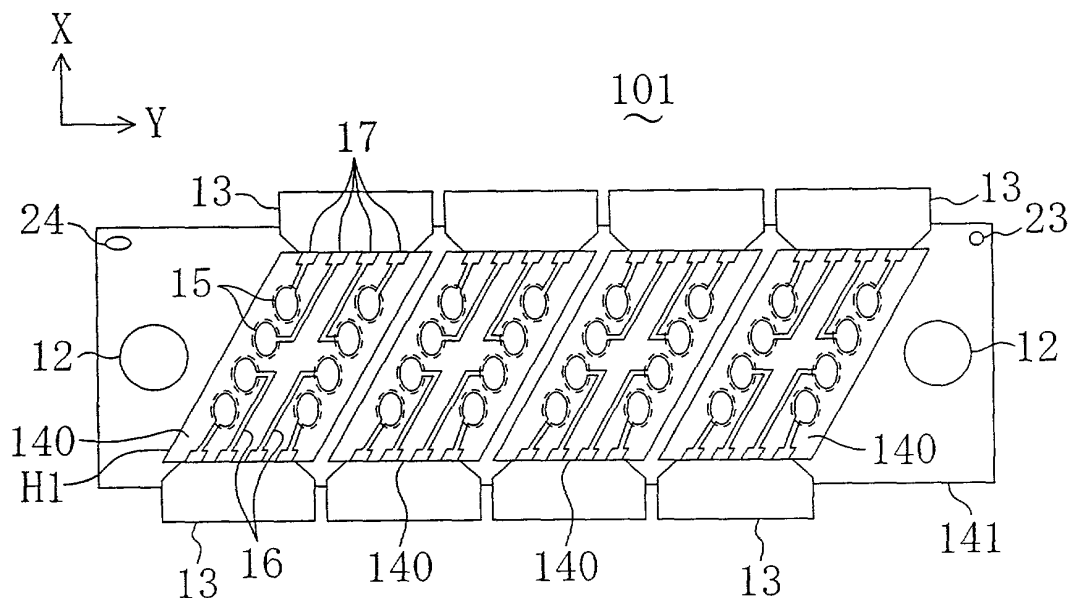


FIG. 17

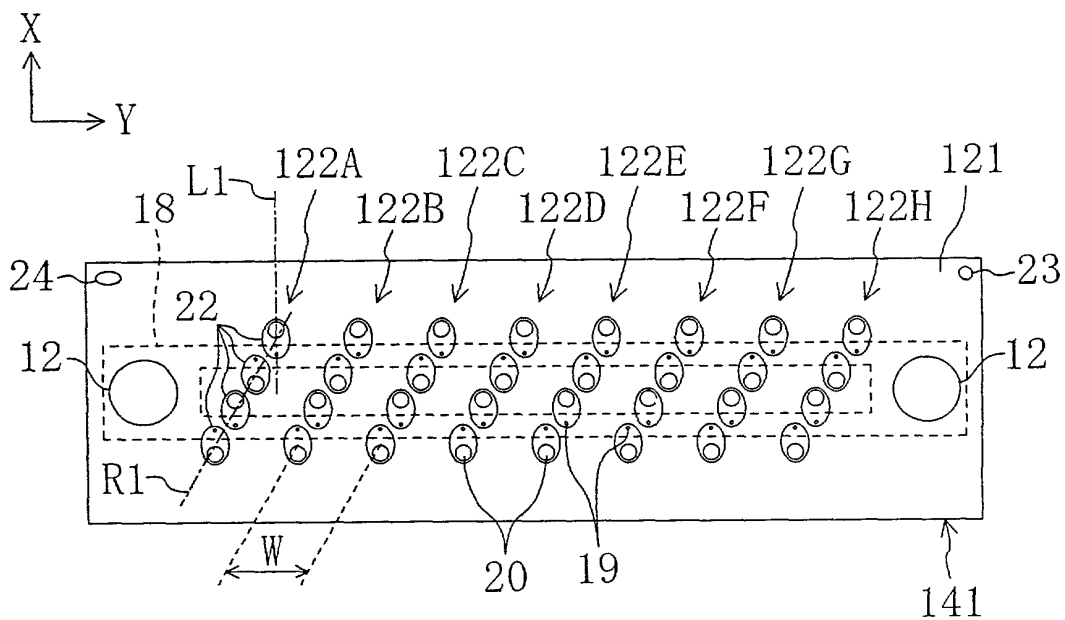


FIG. 18

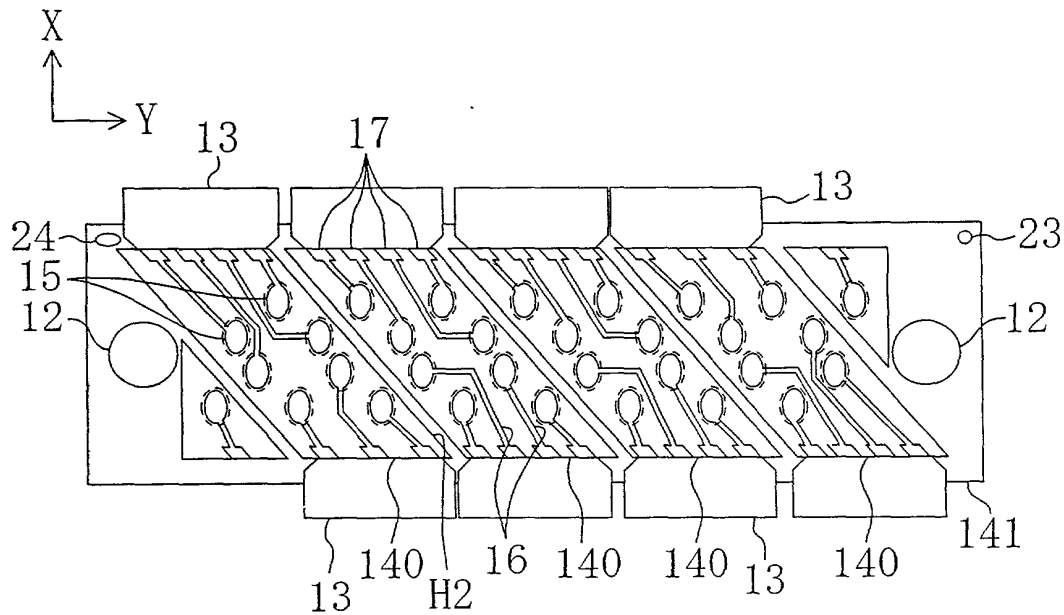
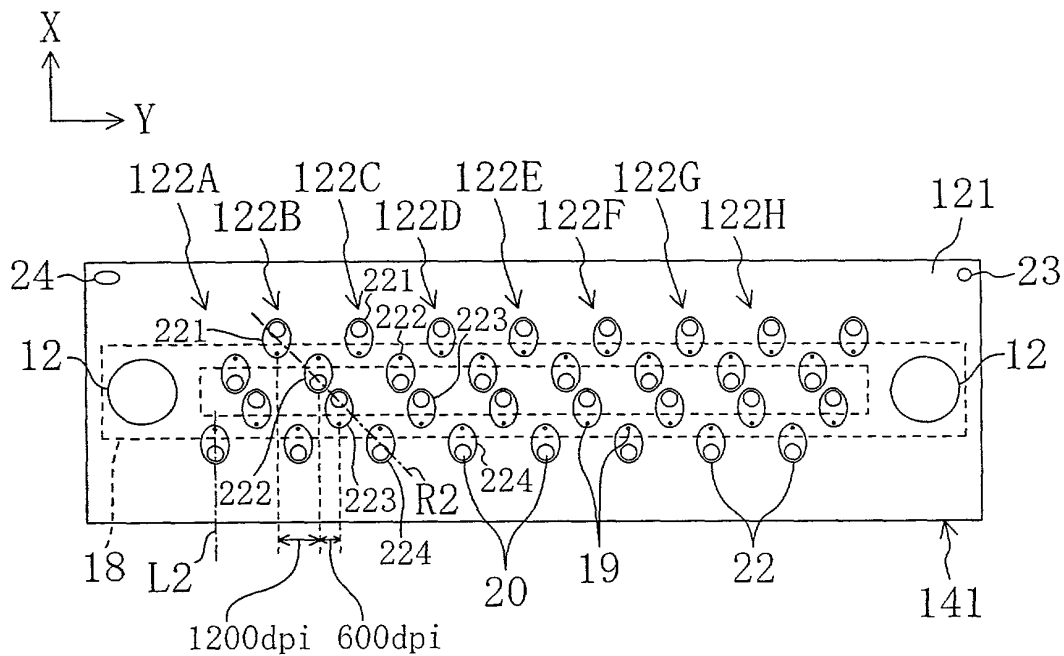
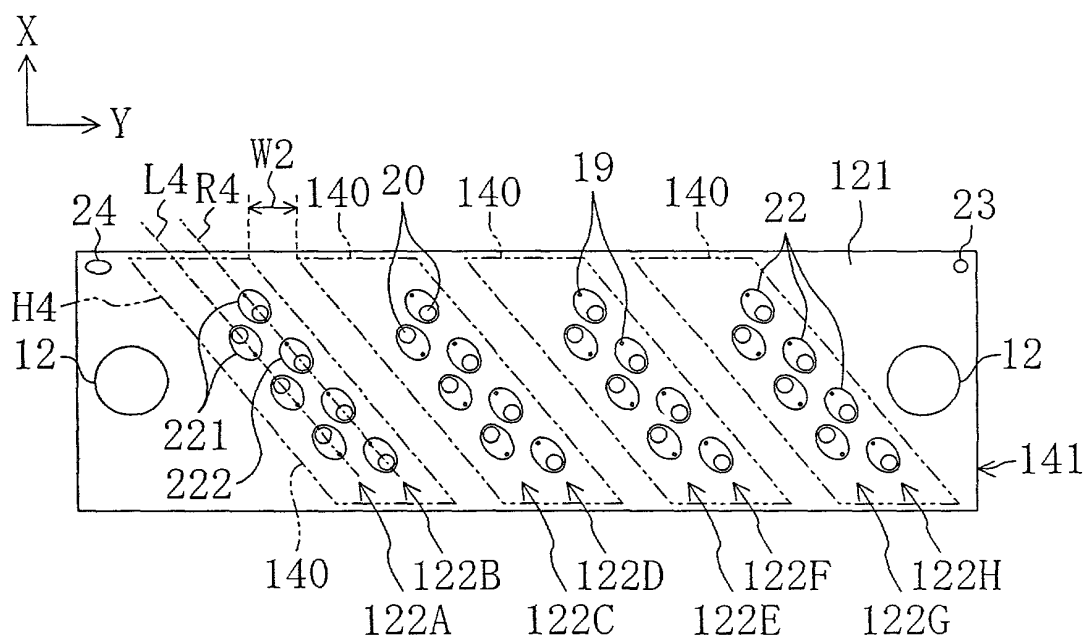


FIG. 19





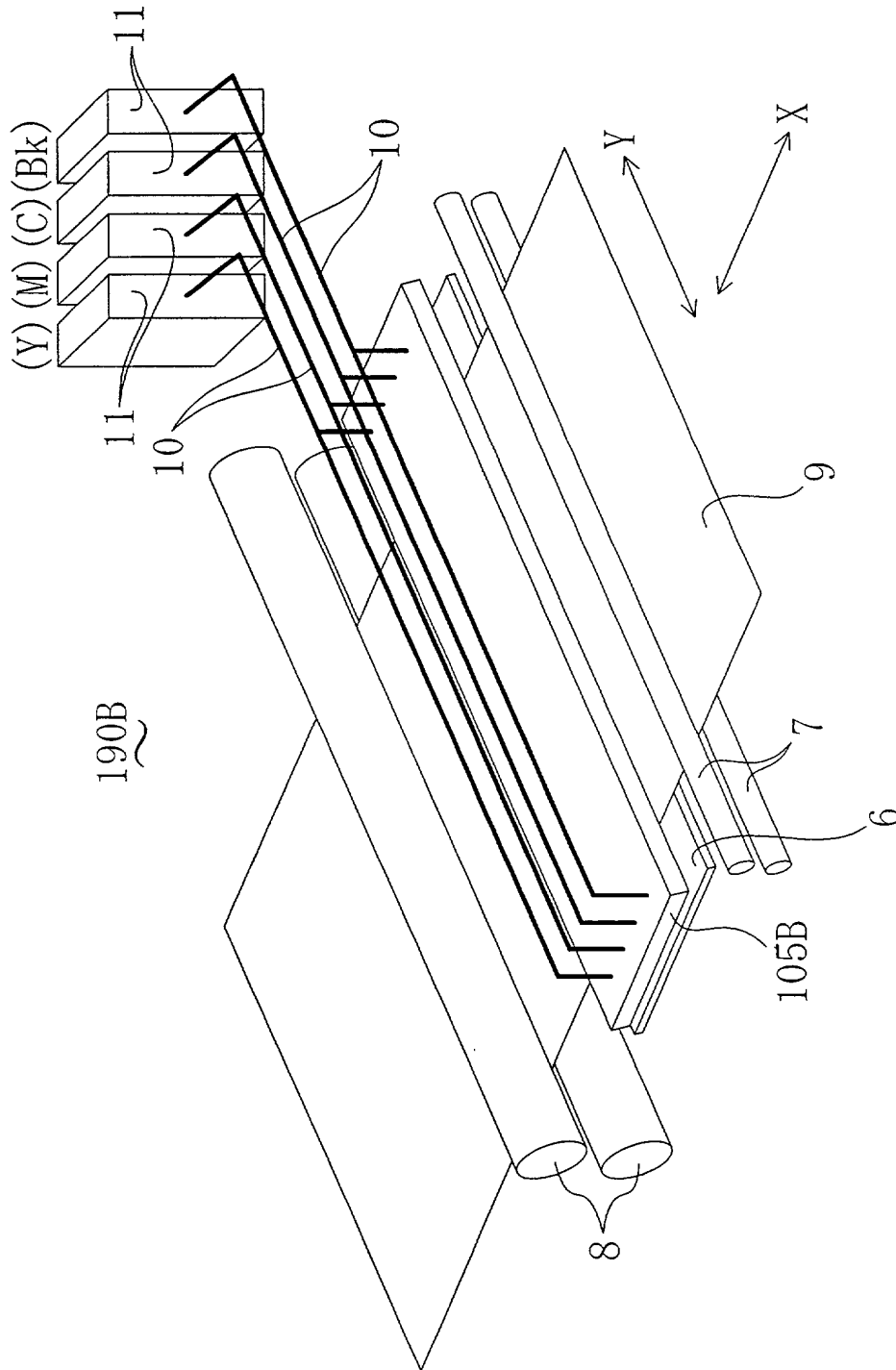


FIG. 23

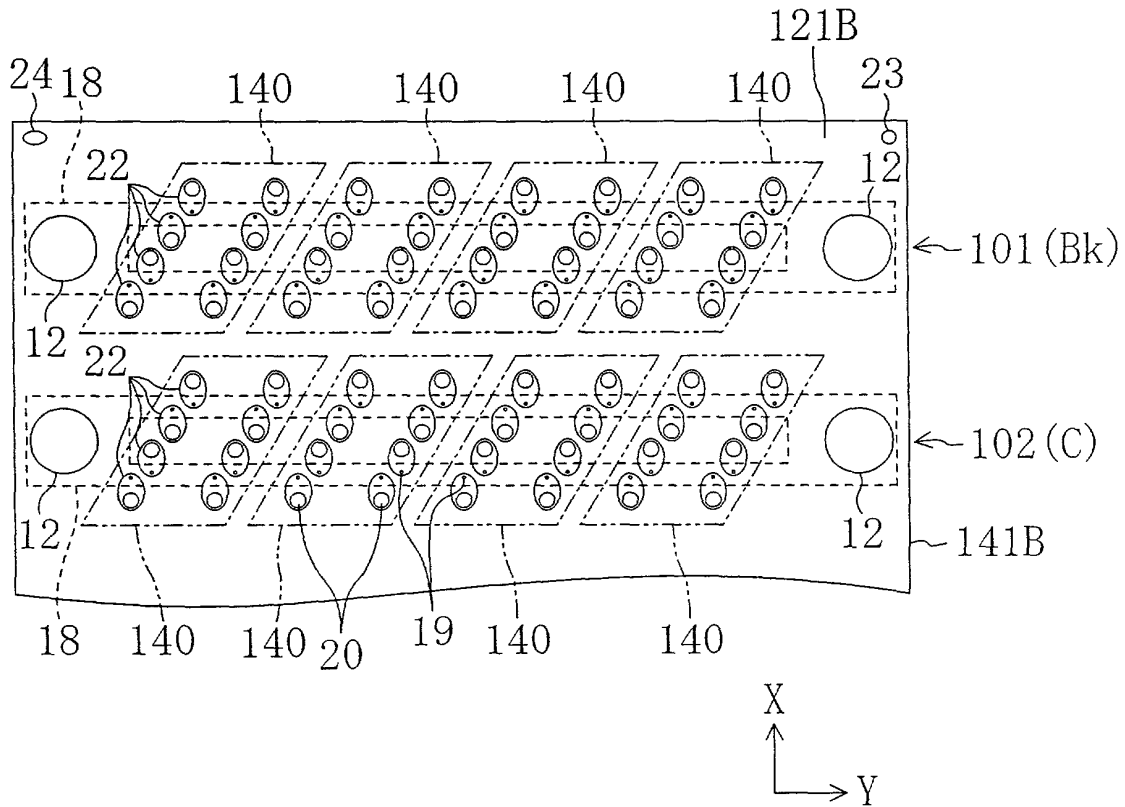


FIG. 24

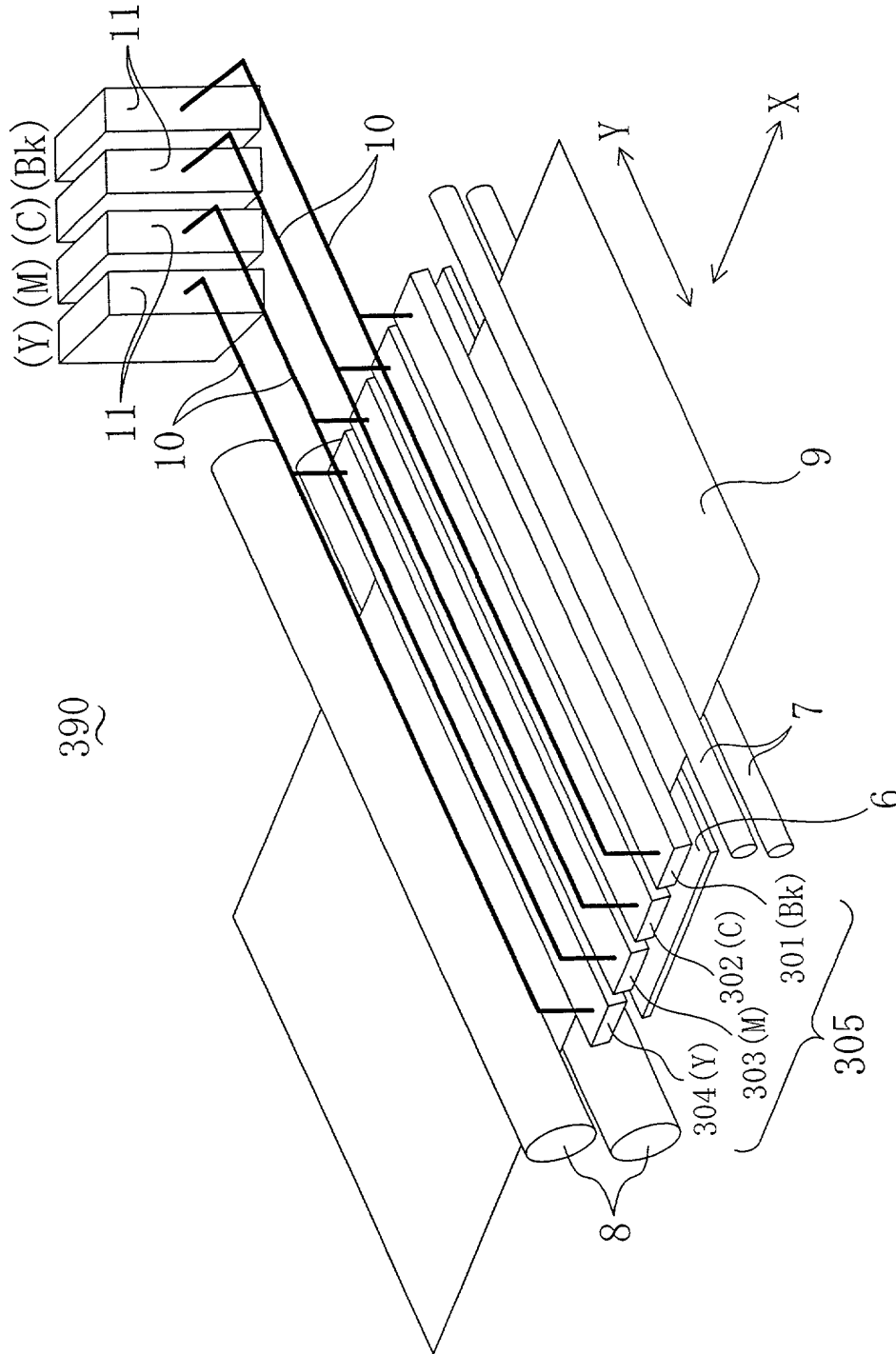


FIG. 25

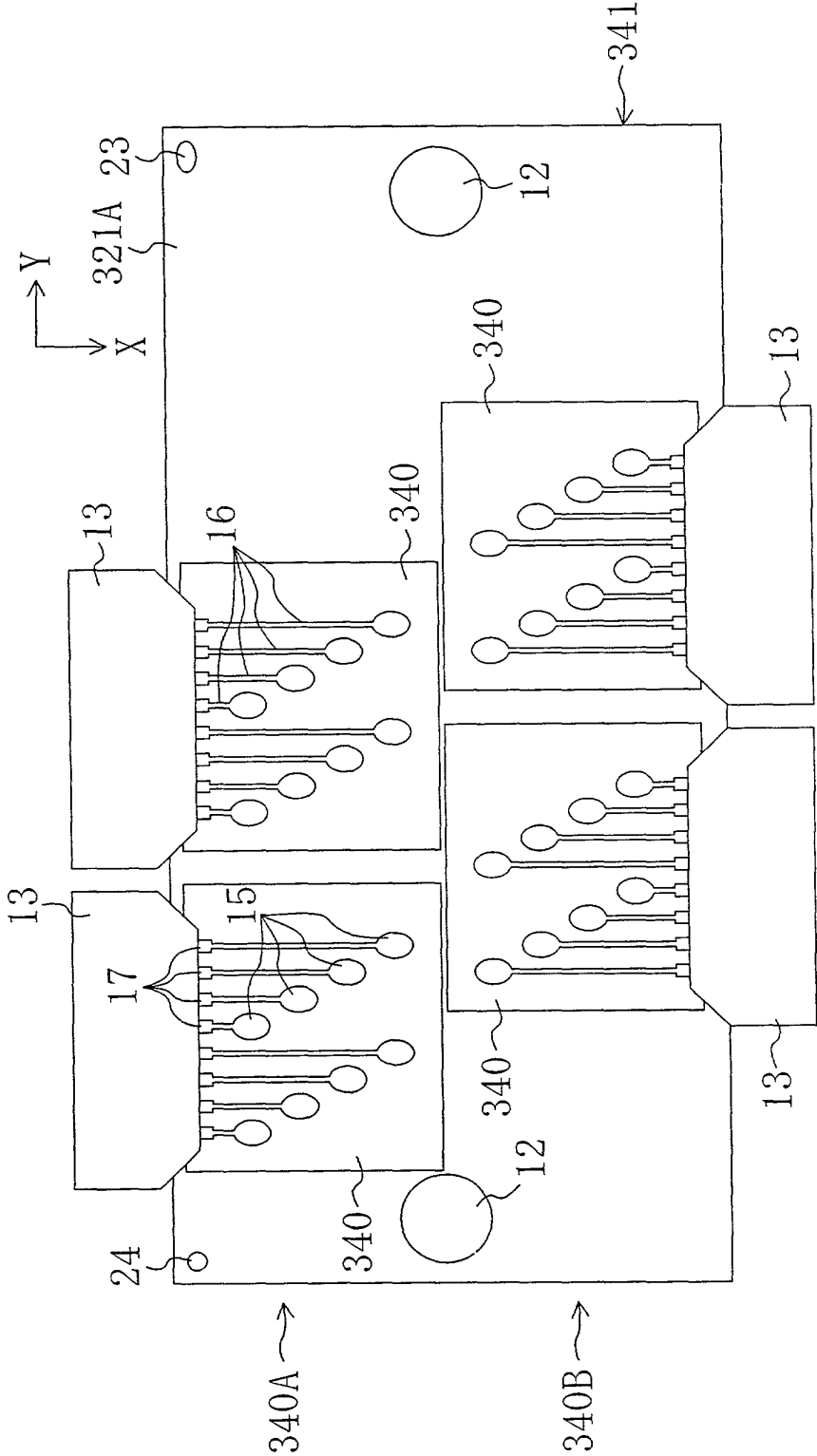


FIG. 26

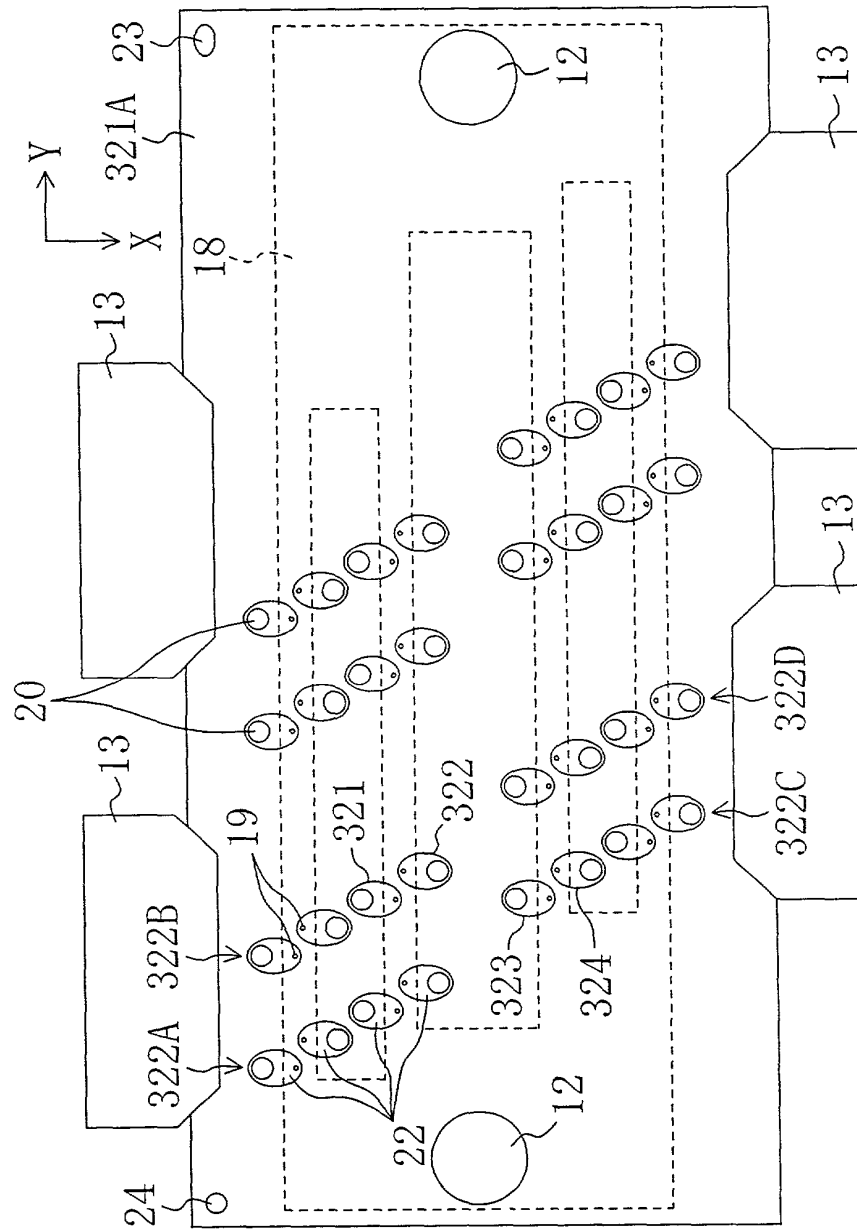


FIG. 27

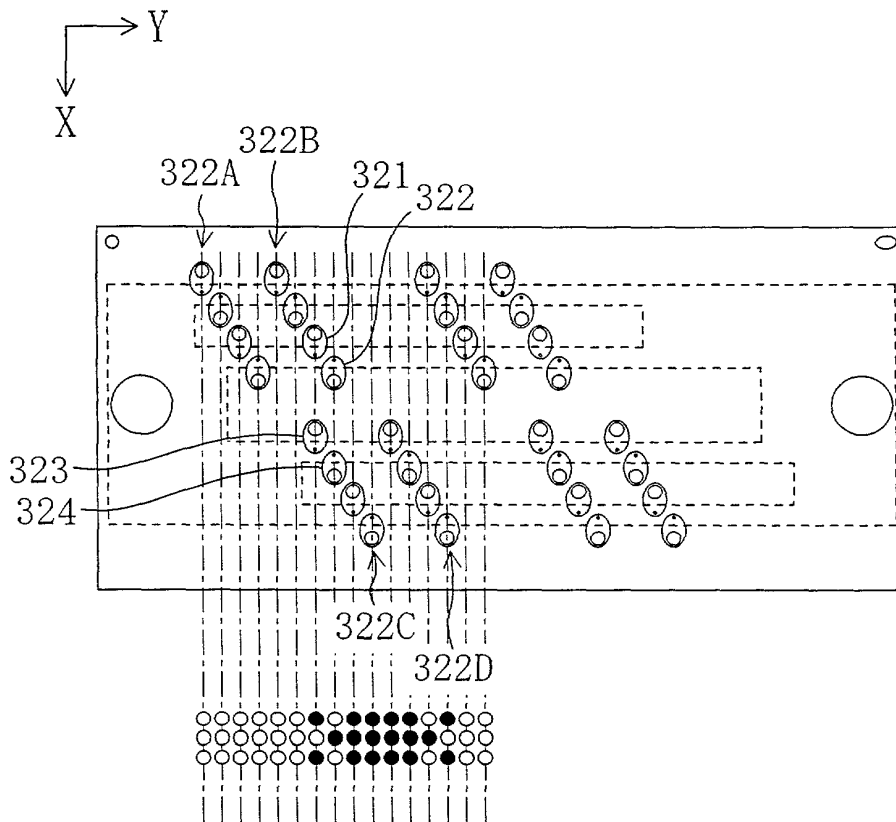


FIG. 28

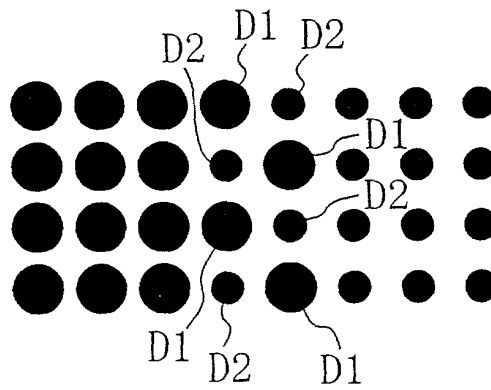


FIG. 29

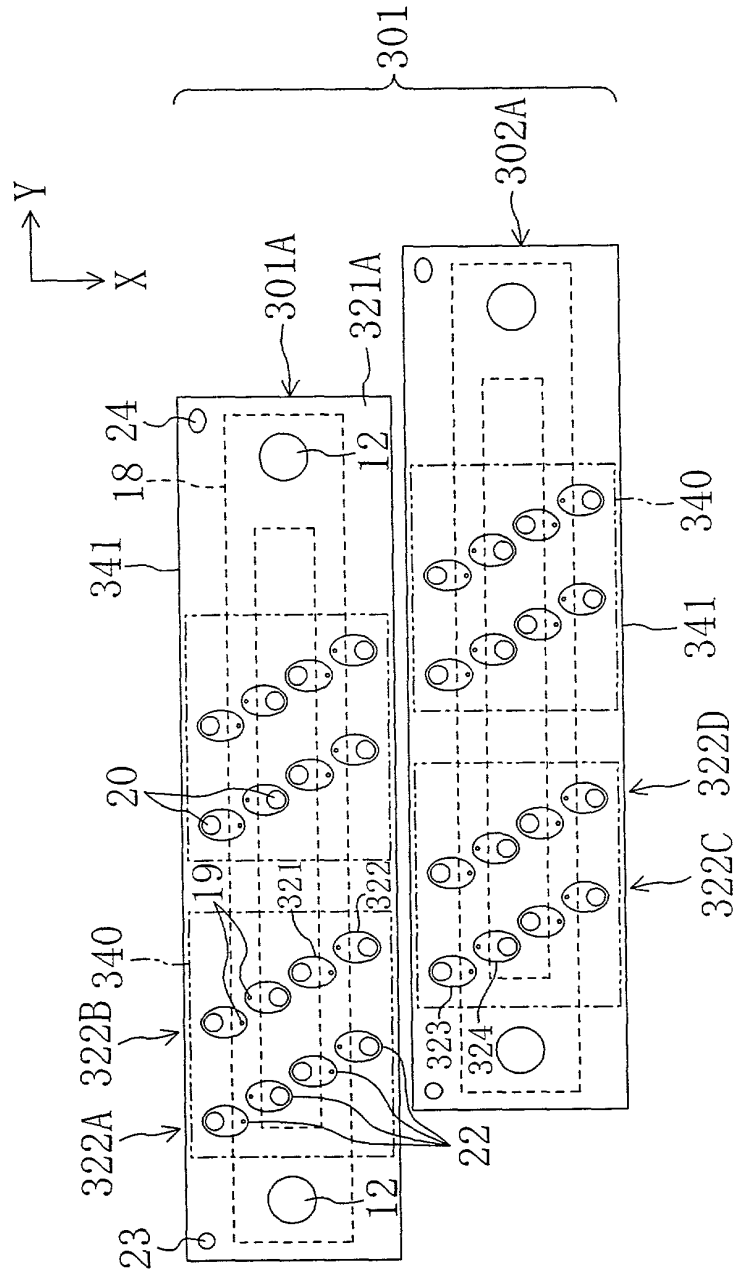


FIG. 30

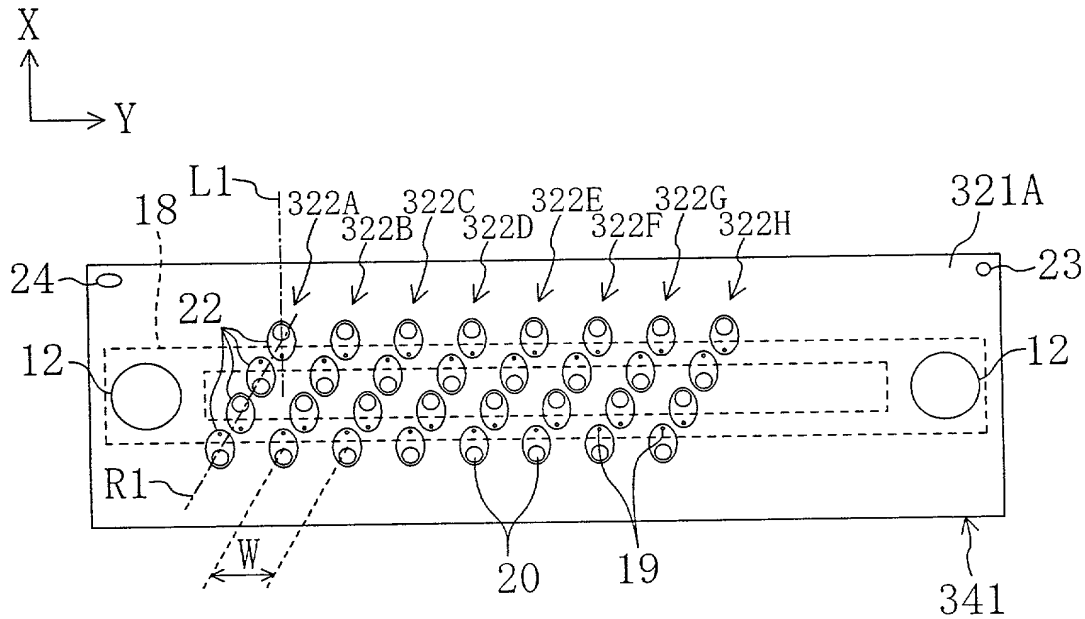


FIG. 31

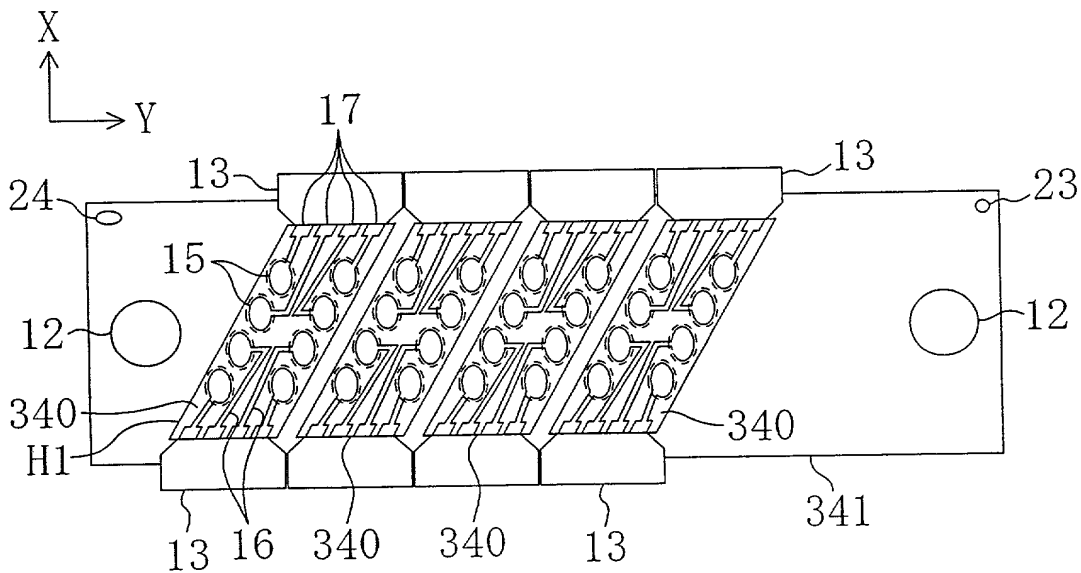


FIG. 32

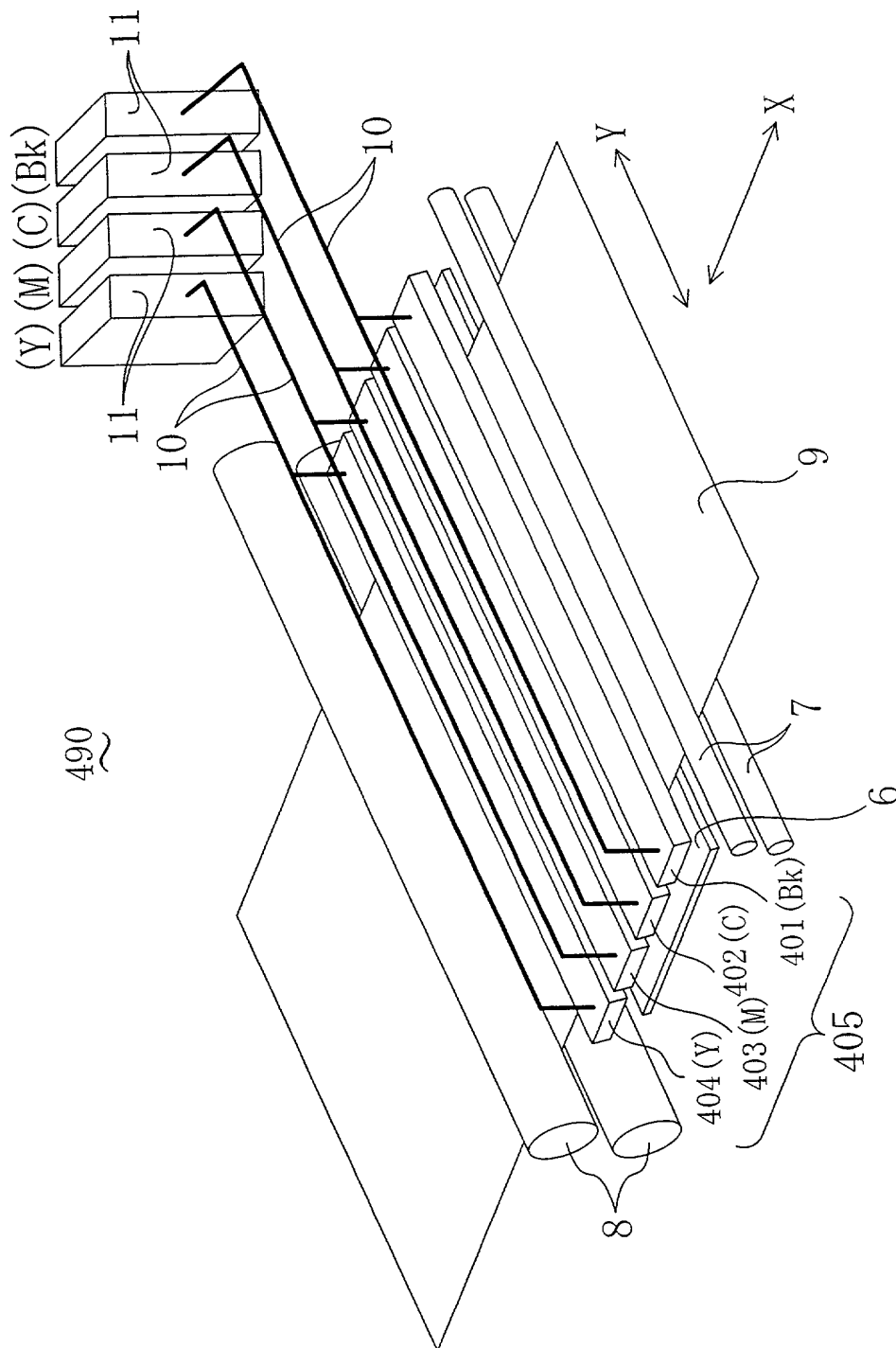
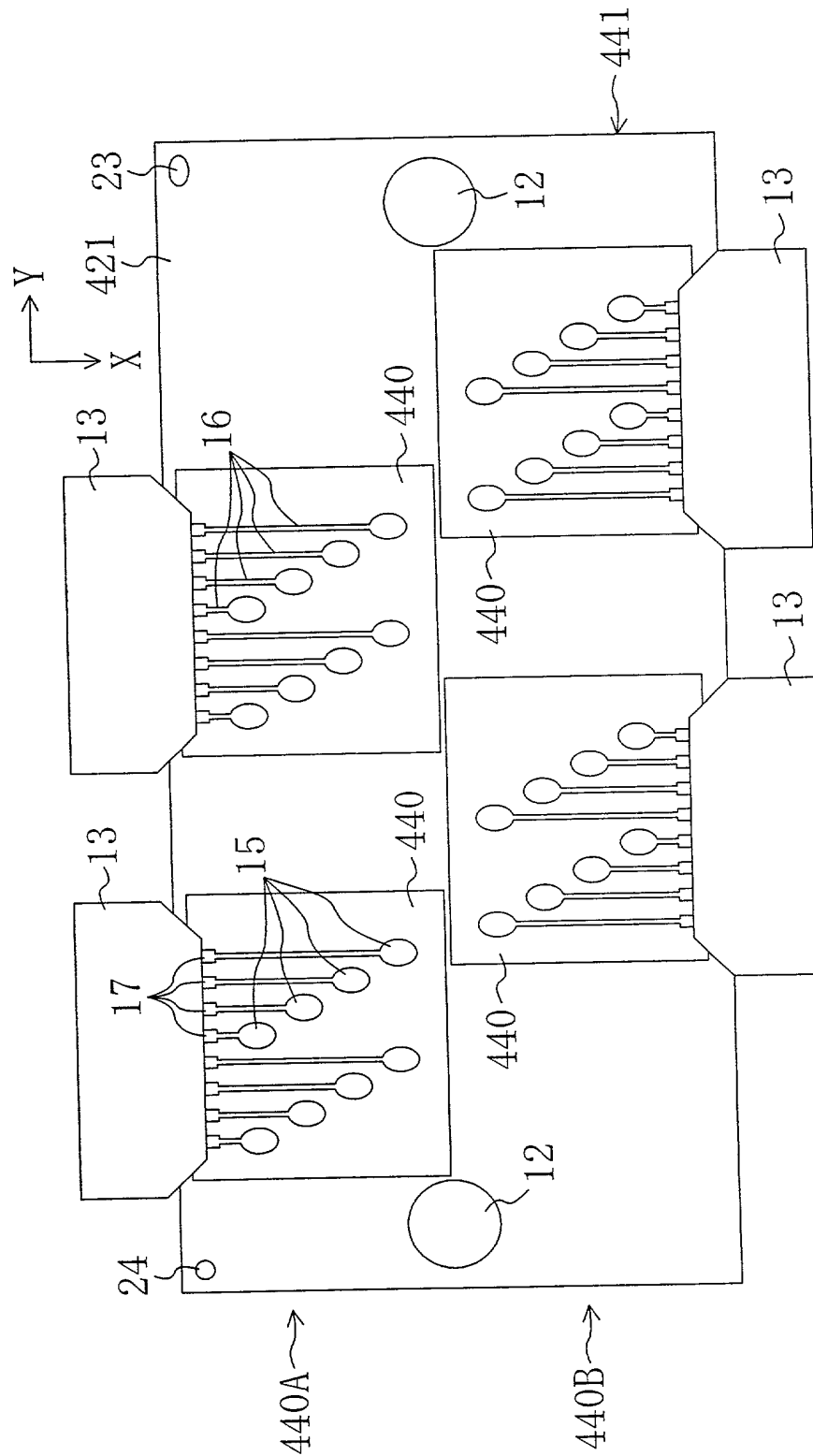


FIG. 33



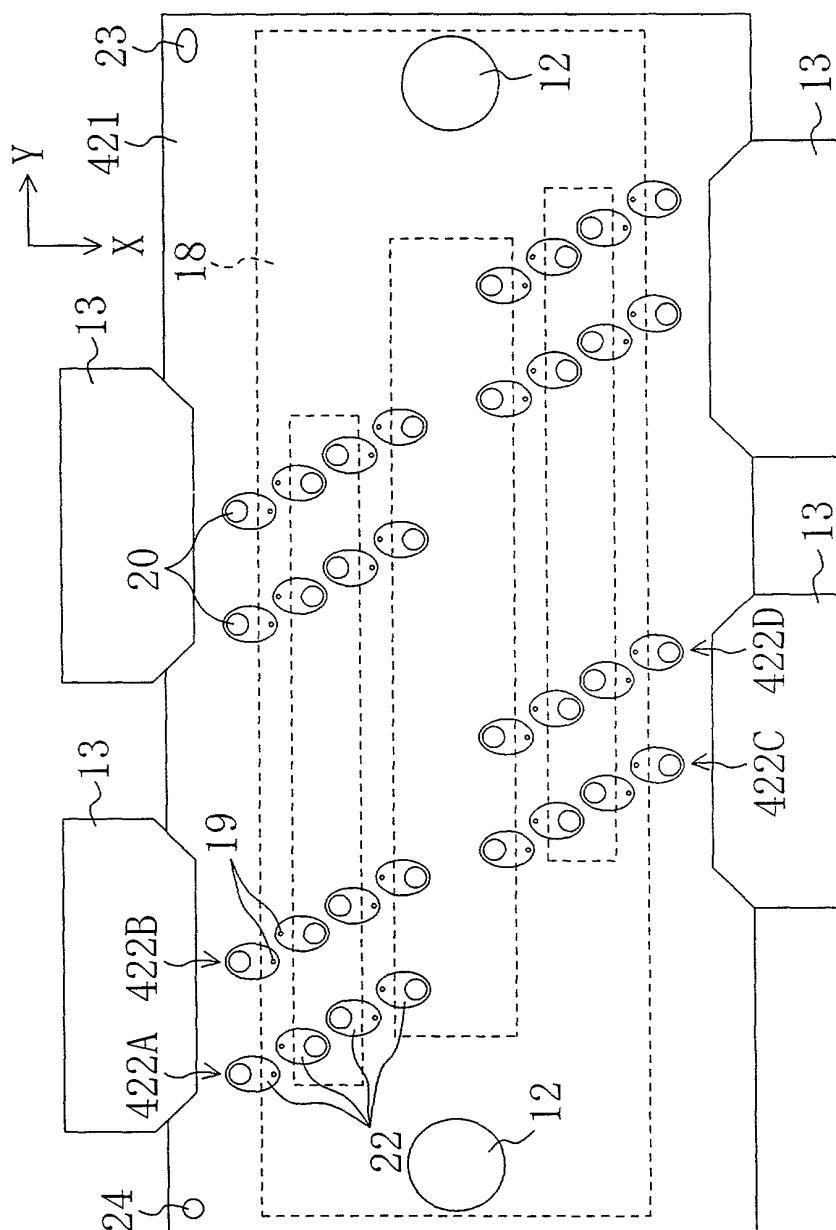


FIG. 35A

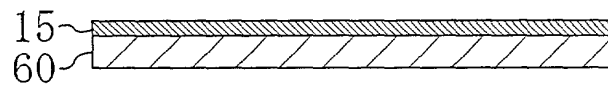


FIG. 35B

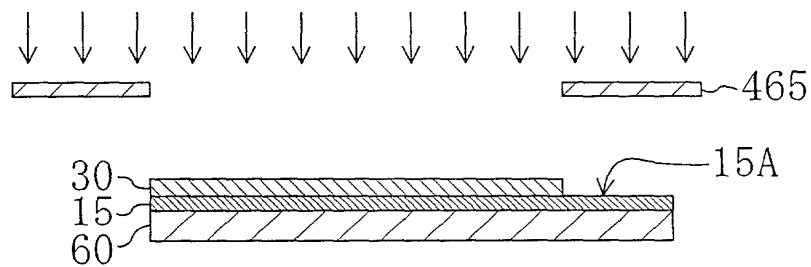


FIG. 35C

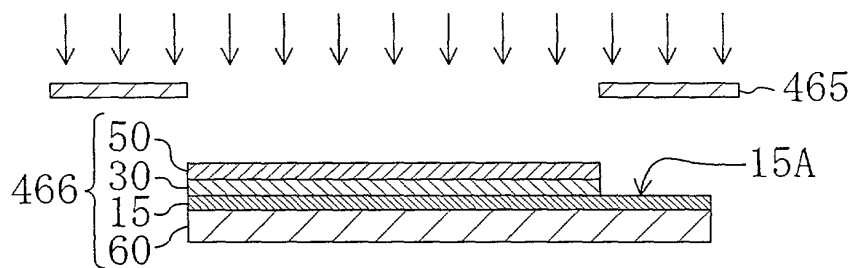


FIG. 36A

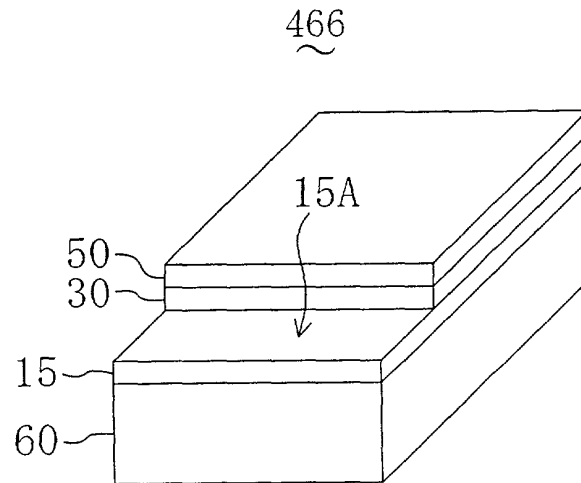


FIG. 36B

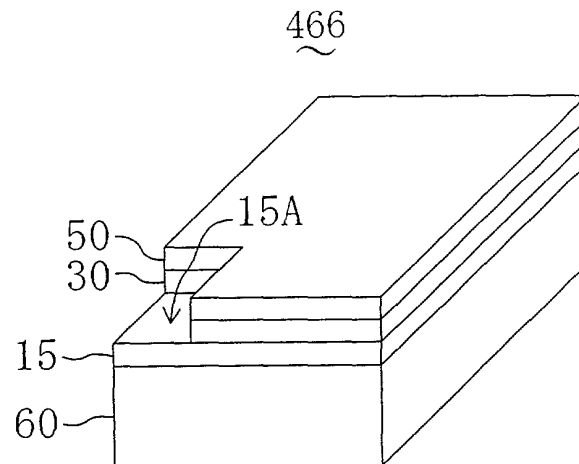
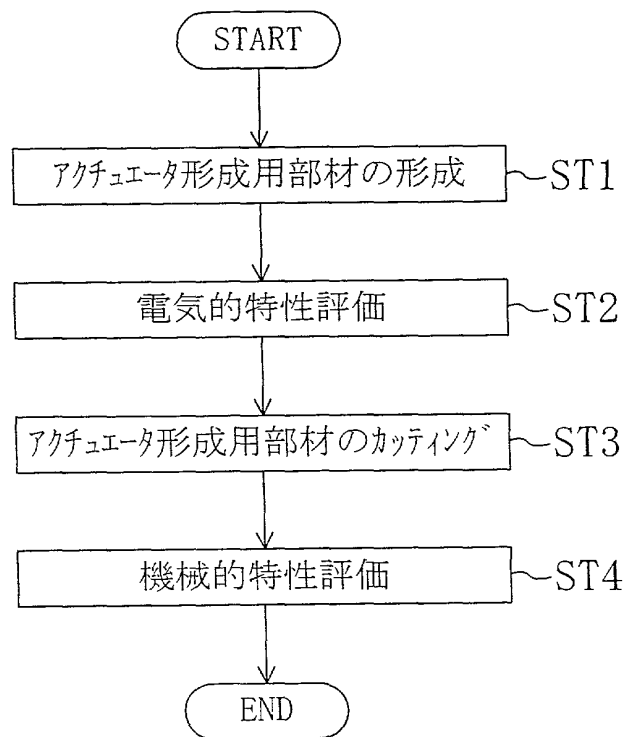
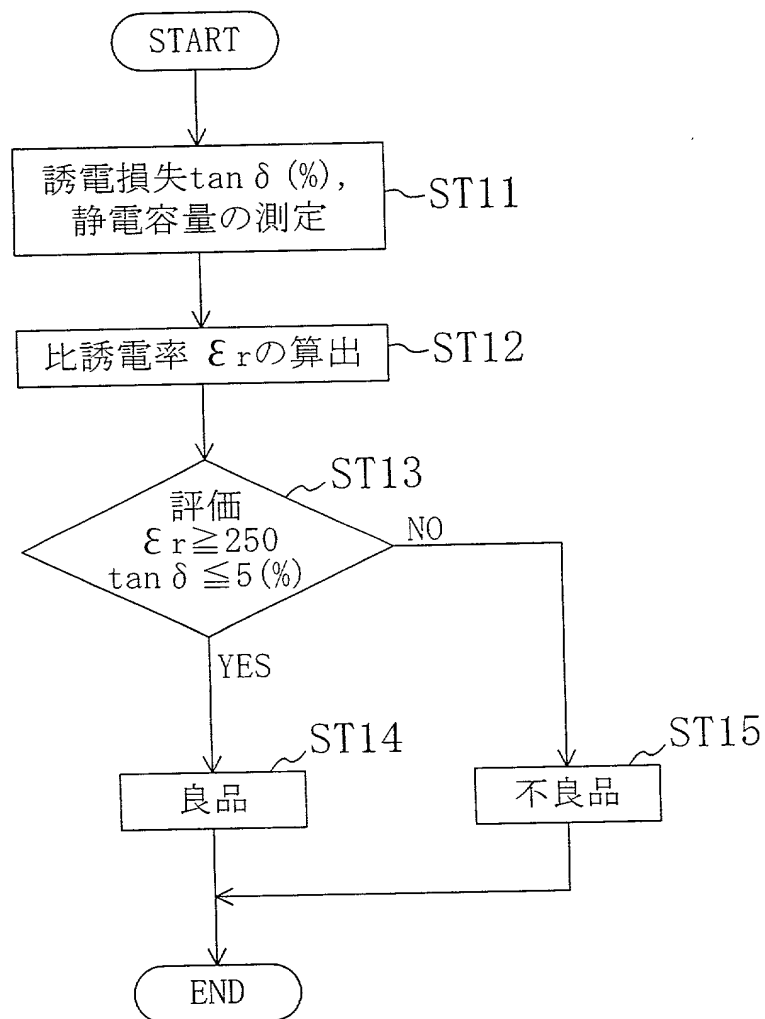


FIG. 37



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FIG. 38



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FIG. 39

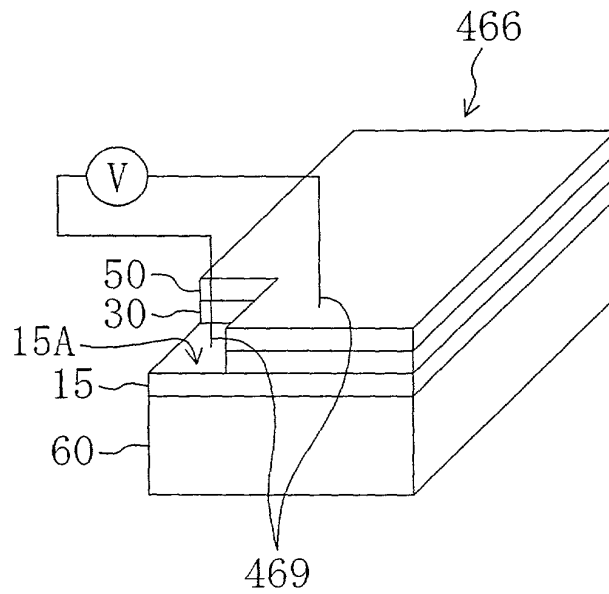


FIG. 40

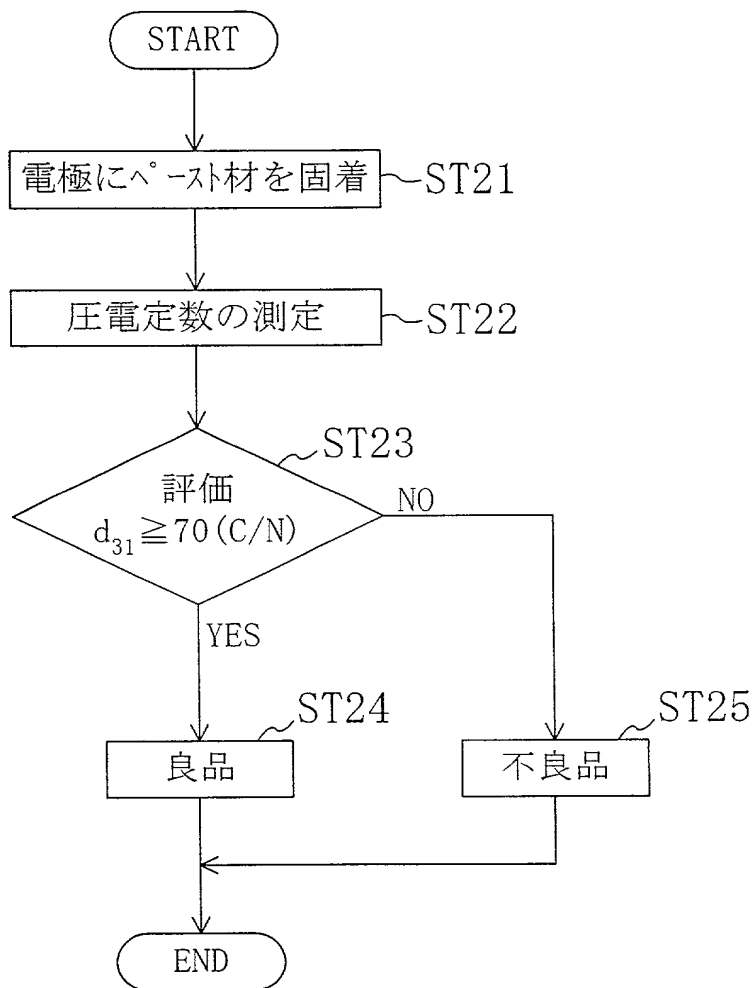


FIG. 41

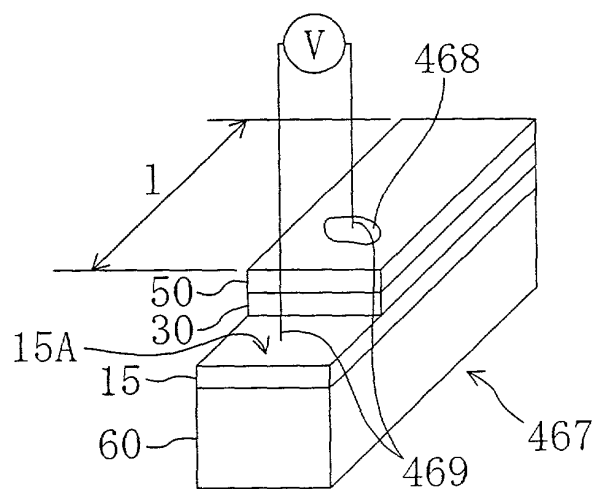


FIG. 42A

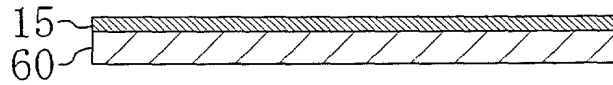


FIG. 42B

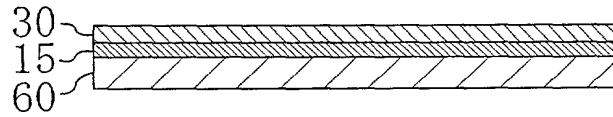


FIG. 42C

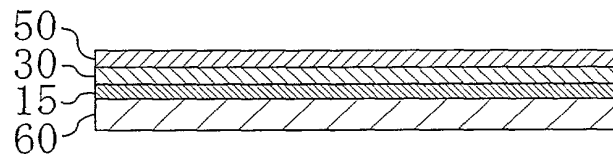


FIG. 42D

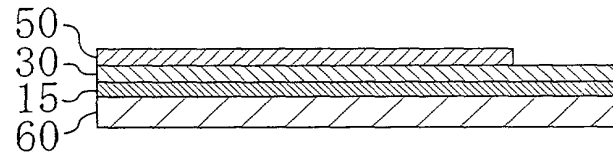
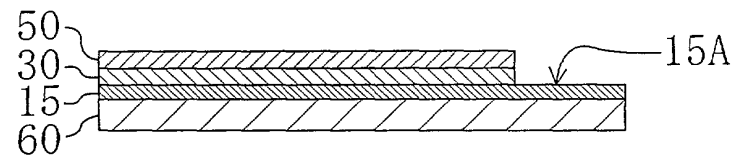


FIG. 42E



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FIG. 43A

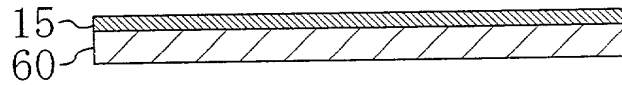


FIG. 43B

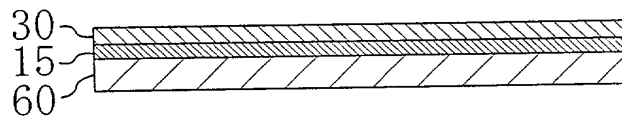


FIG. 43C

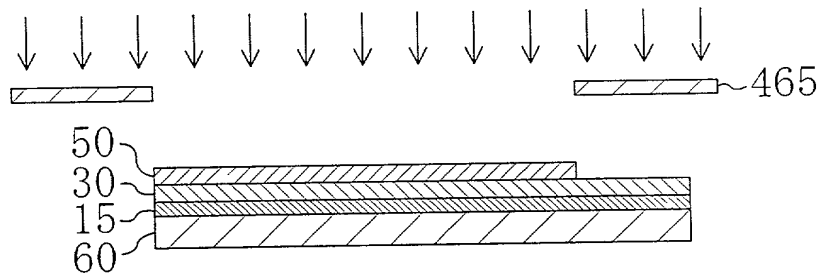


FIG. 43D

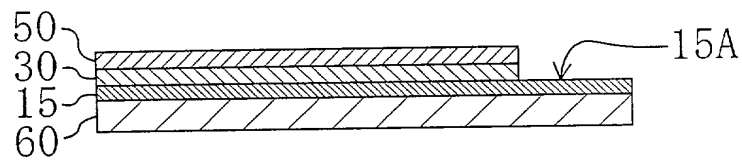


FIG. 44

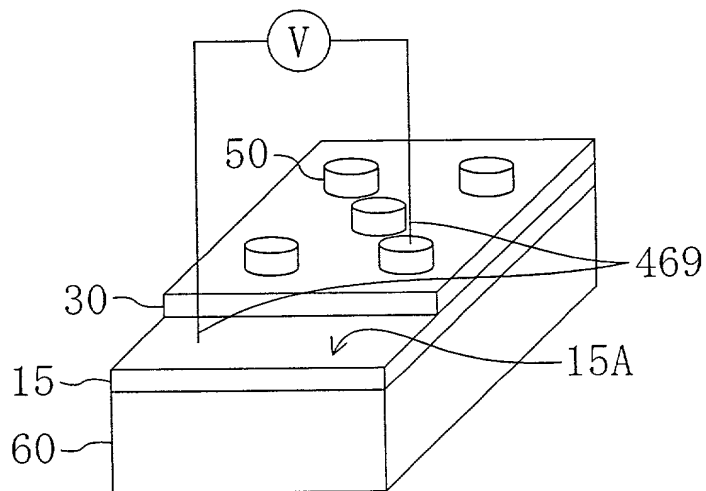
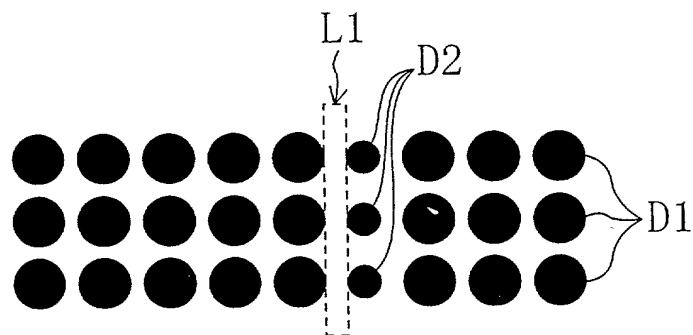


FIG. 45
 Prior Art



United States Patent & Trademark Office
Office of Initial Patent Examination

Application papers not suitable for publication

SN 10,057,279

Mail Date 01-25-02

☒ Non-English Specification

☐ Specification contains drawing(s) on page(s) _____ or table(s) _____

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☐ Handwritten ☐ Specification ☐ Claims ☐ Abstract

☐ More than one column ☐ Specification ☐ Claims ☐ Abstract

☐ Improper line spacing ☐ Specification ☐ Claims ☐ Abstract

☐ Claims not on separate page(s)

☐ Abstract not on separate page(s)

☐ Improper paper size -- Must be either A4 (21 cm x 29.7 cm) or 8-1/2" x 11"

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☐ Non-English text, drawing(s) _____

☐ Excessive text, drawing(s) _____

☐ Photographs capable of illustration, drawing(s) _____

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